Noise analysis and column FPN suppression technology

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Abstract

Noise is an important indicator that affects the image quality. Among the different processing strategies implemented in image sensors, the effect on the noise is complicated. The two types of noise that influences the imaging quality of the digital camera are analyzed firstly. The optical signal and reset signal of the typical correlated double sampling (CDS) are read out through two column amplifiers (CA), respectively. The performance of the two column amplifiers are not exactly the same, resulting in itself will bring the column FPN. To suppress the column FPN effectively, a single amplifier CDS scheme is proposed, which have only one CA, the power consumption and area of the proposed CDS circuit is reduced by half.

Keywords: *Column FPN, Correlated double sampling (CDS), Column amplifier (CA), Denoising.*

1 Introduction

In recent years, rapid research and development have helped the digital imaging device's application more and more widely. The high-quality image acquisition referred to as the focus of attention. Among the different processing strategies implemented in image sensors such as motion detection, feature extraction and adaptive dynamic range enhancement, the effect on the noise are complicated. However, in modern imaging systems, acquired images pass through many stages of digital processing, which can introduce different noise. Acquired images form image sensors are disturbed by kinds of noise interference [1]. Image sensors are characterized as active pixel sensors and passive pixel sensors depending on the readout circuit [2], they incorporate an amplifier in each pixel and amplifying the collected charge outside the array, respectively. However, a variation caused by mismatch in the cell circuit or in the column readout circuits mean that the sensors suffers from fixed pattern noise that degrades the quality of the resulting image. Therefore denoising is particularly important.

In section 2, different noise caused by many stages, such as processing strategies implemented in image sensors and different stages of image processing is discussed. The correlated double sampling circuit with single column amplifier is proposed in section 3. Finally, conclusion is given in section 4.

2 Noise analysis

The imaging process of digital camera image includes two steps, that is, image sampling and image processing. The optical signal collected from optical lens is converted into electric signal through the image sensor in the image sampling process. Through the analog front-ends: the correlated double sampling (CDS), the programmable gain amplifier (PGA) and the digital-to-analog (ADC), the electric signal can be converted into digital signal, that is, mosaic image. The acquired mosaic image is then processed by image processing, which are demosaicing, denoising, enhancing, color correction and so on. The algorithms used in the two stages are complex, several processes are nonlinearity and the effect of different process on the noise is complicated. However, the noise that affecting the image imaging quality consist of two parts, which is caused in the process of the image sampling and the image processing, respectively. There are denoising 1 and denoising 2 of Fig 1.

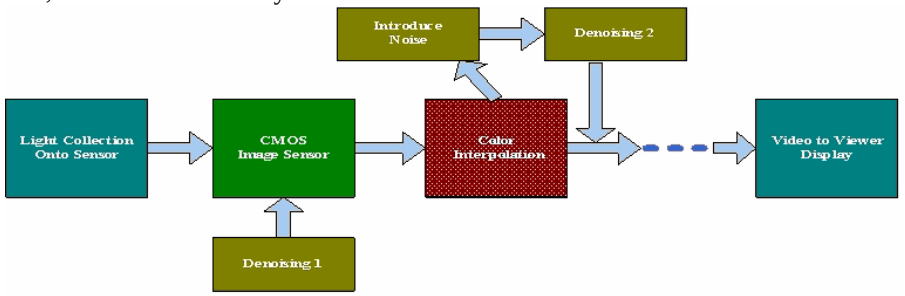

Fig.1 Imaging flow chart

Denoising 1 is processed the noise caused by the image sensor. The image sensor noise can be divided into two categories, the pattern noise and the random noise. The random noise is obvious in the case of low light, which includes thermal noise, KTC noise, dark current shot noise and 1/f noise. The pattern noises include two types, that is, fixed pattern noise (FPN) and photo response non uniformity (PRNU). The latter is related to the illumination pattern noise component, which is independent of time, associated with the signal. Fixed pattern noise is one of the primary limitations to image quality in image sensors, caused by the mismatch between individual pixels or columns of the image sensor, and had much greater effect than the random noise. It is spatial in nature and ideally does not change with time for a particular imager. Two types of FPN have been reported, namely, pixel FPN, which is caused by a mismatch in the cell circuit, and column FPN, caused by a mismatch in the column readout circuits. The main problem of column FPN in an image is not its actual magnitude, but its perceptual effect observed by the human visual system, column FPN can be observed as vertical stripes in an image that are visible even if the magnitude of the column FPN is much lower than the pixel FPN, that is, the column FPN is much more visible than pixel FPN [3, 4]. Although it is hard to quantify the perceptual difference between pixel and column FPN, it has been proposed [5] that random column FPN is five times more harmful to the perceived image quality than pixel FPN. So the column FPN degrades the quality of resulting image, we should reduce it endeavor. Snoeij et al [6] proposed a dynamic column FPN reduction technique, which make the initial column FPN of 0.69% of full scale is made nearly invisible in the measured images.

The target of denoising 2 is the noise caused by the step of image processing, which include the change of the noise structure caused by the demosaicing process and the noise caused by the order of demosaicing and denoising. The influence of demosaicing algorithms on the effects of denoising has been discussed [7]. In the case of noise exist, the demosaicking process will sharpening zoom high-frequency noise, causing noise pollution, changing the structure of the input noise, and forming pseudo-edge, caused the noise analysis becomes very complicated.

3 Correlated Double Sampling Circuit

Nixon et al [7] proposed a typical double sampling circuit to reduce the fixed pattern noise. The pixel FPN is reduced by reading out the pixel and reset signals to the column amplifier (CA). The column FPN is eliminated by reading out the output signal of the column amplifier and the compensation signal to the output column amplifier. The optical signal and reset signal of the typical CDS go through two CA, respectively. The performance of the two column amplifiers are not exactly, resulting in itself will bring the column FPN. To suppress the column FPN, a switch was added in the two paths of the optical signals and reset signals [9], sampled once when the effective optical signals were read-out. The method can reduce the column FPN effectively, with the cost of add once sampling and increase the power consumption. The column FPN can be observed as vertical stripes in an image that seriously affecting image quality. In order to effectively reduce FPN column, the paper introduces a design scheme of single amplifier CDS, as shown in Fig 2.

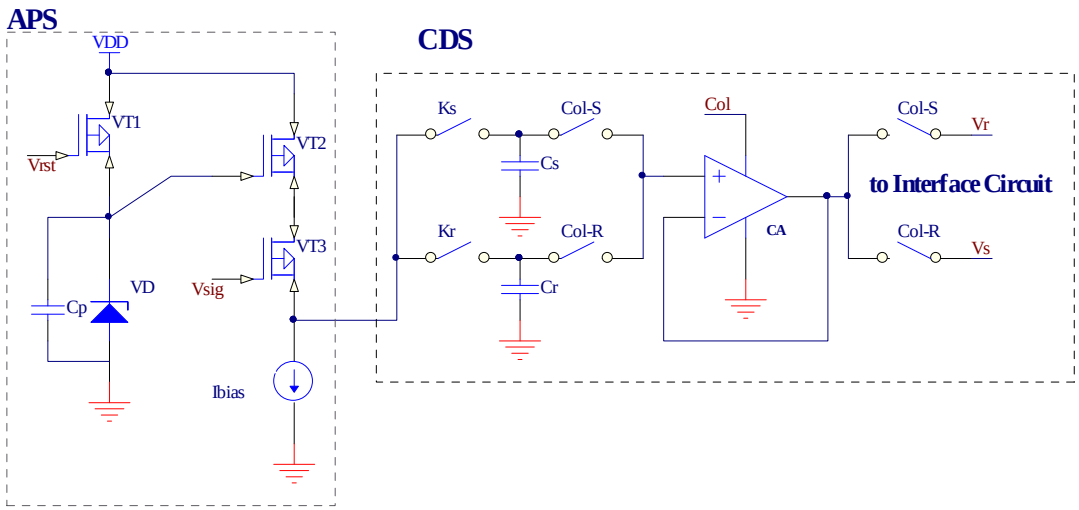

Fig 2 The proposed single amplifier CDS

There is only one single column amplifier in Fig 2, so the readout signal from APS should be sampling twice. That is, sampling the optical signal V_{sig} to C_s using K_s, then, sampling the reset signal V_{rst} to C_r using K_r. Finally, the effectively optical signal V_{opt} can be obtained with the subtraction of V_{sig} and V_{rst}. Since these two values are read out through the same path, the column FPN is greatly reduced in one difference operation, so that it can be ignored.

The workflow of the proposed single amplifier CDS circuit can be described in two steps:

(1) Sample. Sampling the optical signal V_{sig}, in this process, *Col_S* is effectively, the node voltage value of V_s can be gotten with the following equation.

$$V_S(n) = V_{stg} + \Delta \quad (1)$$

(2) Hold. Sampling the reset signal V_{rst}, in this process, *Col_R* is effectively, the node voltage value of V_r can be gotten with the following equation.

$$V_r(n+1) = V_{rst} + \Delta \quad (2)$$

The effectively optical signal V_{opt} can be obtained from equation (1) and equation (2), that is, the difference operation of them, the result as follows.

$$V_{opt}(n) = V_r(n+1) - V_S(n) = V_{rst} - V_{stg} \quad (3)$$

In which, Δ is the column FPN caused by the column amplifier.

Compared with the traditional CDS circuit, there is only one CA in each column, so the power consumption and area of the proposed CDS circuit is reduced by half. The optical signal V_{sig} and the reset signal V_{rst} are read out through the same path, the column FPN is greatly reduced, so that it can be ignored. The results of the proposed scheme are compared with the algorithms of [8] and [9], which can be seen in Table 1. Obviously, the column FPN of the proposed scheme greatly reduced, both power consumption and area decreased as well.

Table 1 the compare results

	[8]	[9]	the proposed
area	small	small	small
power consumption	big	moderate	small
column FPN	moderate	big	small

3.1 Single Column Amplifier

The most simple column amplifier is source follower, which has great influence by the manufacture process, and has poor output linearity. So, the op-amp is generally used to take the place of column amplifier, and has been widespread in many fields.

Symmetrical operational transconductance amplifier (OTA) is widely used for the wide swing, big gain bandwidth product, the input and output can be shorted at the same time. Fig 3 is the traditional symmetrical OTA [10]. In it, *Col_sel* is column choose signal, p_{bisa} is offset voltage, V_i is input, V_o is output. We use it as the single column amplifier in the proposed correlated double sampling circuit.

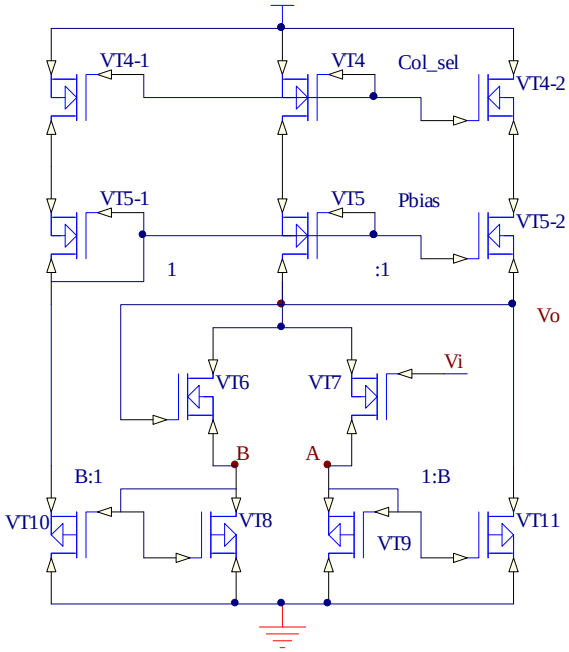

Fig.3 The traditional symmetrical OTA

3.2 Interface Circuit

The proposed CDS circuit can not output the optical signals and the reset signals simultaneously, can not connected with PGA directly, because there is only one CA. So it is necessary to design an interface circuit, as shown in Fig 4. The OTA in it is symmetrical operational transconductance amplifier, which has been introduced in the last part. The node voltage V_s and V_r are the input of the interface circuit, which have the same meaning with Fig 2. V_o is the output of the interface circuit, which connected with PGA.

The working principle of the interface circuit is presented below.

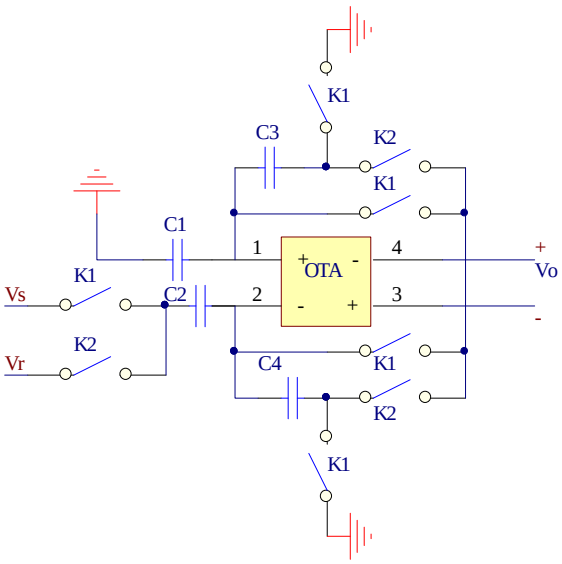

Fig 4 The interface circuit between CDA and PGA

Firstly, clock S_1 effective, sampling the optical signal V_{sig} and preserve it to C_2.

Then, disconnect S_1, clock S_2 effective, sampling the reset signal V_{rst}, and subtract the optical signal V_{sig} at the same time.

Thus, the output signal V_{rst} -V_{sig} can be obtained, which is the output of interface circuit and connected with PGA, the result can be gotten with the following equation.

$$V_o == V_{rst} - V_{stg} \quad (4)$$

5 Conclusions

Denoising and demosaicing are two important aspects of the image imaging process. The noises affecting image imaging quality consist of two parts, which are image sensor noise caused in the process of the image sampling and the noise caused by demosaicing. The proposed CDS technology used one CA to read out optical signal and reset signal sequential, can greatly suppress the column FPN of the image sensor noise. The power consumption and area of the proposed CDA circuit is reduced by half simultaneously.

Acknowledgments

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