Integrated Circuit of CMOS DC-DC Buck Converter with Differential Active Inductor

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Abstract

In this paper, we propose a new design of DC-DC buck converter (BC), which the spiral inductor is replaced by a differential gyrator with capacitor load (gyrator-C) implemented in 0.18um CMOS process.

The gyrator-C transforms the capacitor load (which is the parasitic capacitor of MOSFETS) to differential active inductor DAI. The low-Q value of DAI at switching frequency of converter (few hundred kHz) is boosted by adding a negative impedance converter (NIC).

The transistor parameters of DAI and NIC can be properly chosen to achieve the desirable value of equivalent inductance L (few tens µH), and the maximum-Q value at the switching frequency, and thus the efficiency of converter is improved.

Experimental results show that the converter supplied with an input voltage of 1V, provides an output voltage of 0.74V and output ripple voltage of 10mV at 155 kHz and Q-value is maximum (≈4226) at this frequency.

Keywords**:** *DC-DC Buck converter, gyrator-C, differential active inductor, negative impedance converter, quality factor, efficiency.*

1. Introduction

Switching DC-DC converter is ubiquitous in mobile electronic systems. The trend towards low-power dissipation, low voltage, and high accuracy in portable equipments has been driving technology, as well as the parametric requirement of integrated DC-DC converters.

Magnetic theory is at the heart of any non linear regulator with the use of a spiral inductor to transfer energy from input to output in a lossless fashion, and to filter the output from switching signals.

This paper introduces the concept of differential active inductor [1], [2], with high-equivalent inductance value (few µH) and maximum-Q value at switching frequency, thus to allow the complete integration of DC-DC Buck converter, which is especially important in portable power applications.

Section 2 reviews the relevant information of DC-DC buck converter. The realization of the CMOS differential active inductor is presented in section 3, and improved in section 4. The novel concept of buck converter using DAI and NIC is described in section 5. The simulation results obtained on a 1V to 0.74V buck converter are then shown and discussed in section 6. Finally, a conclusion is given in section 7.

2. General view of classical step-down converter in continuous mode

The buck (or step-down) converter is a switching power supply, used to generate a low regulated DC output voltage from higher DC input voltage normally unregulated. [3], [4], [5].

The main components of the BC are a spiral inductor and two switches oppositely phased, that control the storage energy in the inductor, and it's discharging in to the load, Fig.1.

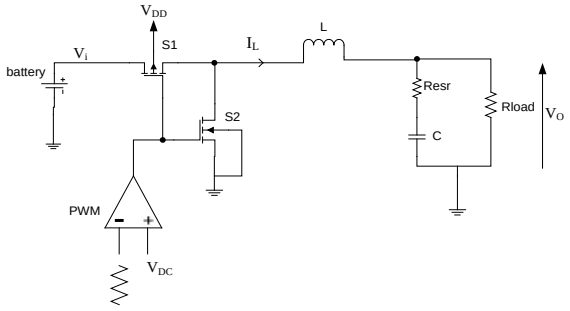


Fig.1 Ideal step down converter.

The switches S_1 and S_2 are usually PMOS and NMOS power transistors driven by a PWM signal at fixed frequency $f_s = \frac{1}{T} = \frac{1}{T_{on}+T_{off}} = \frac{1}{DT+(1-D)T}$, and Varying duty cycle, $D = \frac{T_{on}}{T}$ $0 \le D \le 1$.

The BC operates as follows:

- During T_{on}: switch S_1 is in on-state (closed) and S_2 is in off-state (opened), the inductor is charging, the increase current during T_{on} is giving by:

$$\Delta I_{Lon} = \int_0^{T_{on}} \frac{V_L}{T} dt = \frac{(V_i - V_o)T_{on}}{L} \qquad (1)$$

Where V_i is the input voltage and V_o is the output voltage.

- During T_{off}: switch S_1 is in off-state (opened) and S_2 is in on-state (closed), the voltage a cross the inductor is $V_L = -V_o$, the decrease current during T_{off} is giving by:

$$\Delta I_{Loff} = \int_{T_{on}}^{T_{off}} \frac{V_L}{T} dt = \frac{-V_o}{L} T_{off} \qquad (2)$$

If we assume that the current I_L is the same at $t = nT$ and $t = (n+1)T$, with n an integer.

Therefore:

$$\Delta I_{Lon} + \Delta I_{Loff} = 0$$

$$\Rightarrow \quad \frac{(V_i - V_o)T_{on}}{L} - \frac{V_o}{L} T_{off} = 0$$

$$\Rightarrow \quad V_o = DV_i = \frac{T_{on}}{T} V_i \qquad 0 \le D \le 1$$

The previous study was conducted with the following assumptions:

- The filter capacitor has enough capacitance to keep V_o constant.
- The switches are a very low R_{DSon}.
- Parasitic resistor of inductor is neglected.

3. CMOS differential active inductor

In order to alleviate the limitations imposed on the chip area, and the quality factor (Q) of the spiral inductor, several CMOS active designs were proposed to implement the required on-chip inductance [6], [7].

Fig.2 (a) shows the schematic of the DAI with input $\pm \frac{v_{in}}{2}$ at the source (M_{2a} and M_{2b}) [8], where the pair of stabilizers (M_{3a} and M_{3b}) and negative impedance cross-coupled MOSFET pair (M_{1a} and M_{1b}) have been included at the drain and source of the proposed gyrator circuit respectively. The pair of current sinks M_Q is introducing for external flexible Q tuning, is can be performed by varying I_Q which leads to changes in g_{m1}.

A replica bias circuit M_{L1}, M_{L2} has been introduced to allow current-controlled inductance of the DAI.

Based on a first order small signal analysis, the equivalent RLC circuit of this inductor is shown in Fig.2 (b).

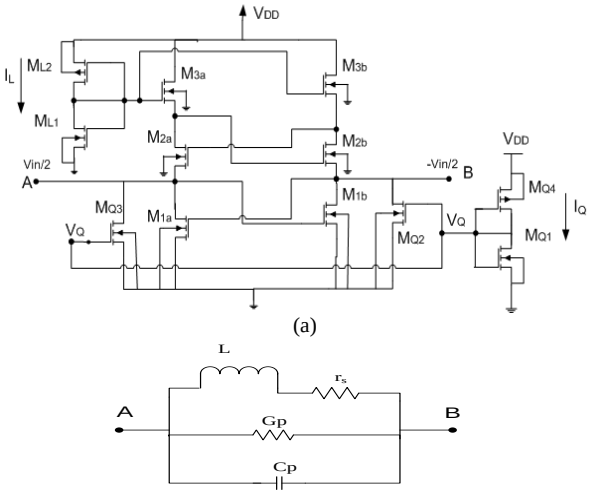


Fig. 2 (a) Differential active inductor, (b) equivalent RLC model of DAI

The input admittance of the DAI is given by:

$$Y_{in} \approx pC_1 + (g_{m2} - g_{m1} + g_{Q3} + g_1 + g_2) + \frac{g_{m2}^2}{(g_{m3} - g_{m2} + g_2 + g_3) + pC_2} \qquad (3)$$

With $C_1 = C_{gs2} + C_{gs1}$

$C_2 = C_{gs2} + C_{gs3} + C_{bd2} + 2C_{gd2}$

Where g_m and g are the transconductance and output conductance of the corresponding transistors.

Neglecting the gate-drain capacitance, we have:

$$L \approx \frac{C_{gs2} + C_{gs3} + C_{bd2}}{g_{m2}^2} \qquad (4)$$

$$r_s \approx \frac{g_{m3} - g_{m2} + g_2 + g_3}{g_{m2}^2} \qquad (5)$$

$$C_p \approx C_{gs2} + C_{gs1} \qquad (6)$$

$$G_p \approx \frac{1}{g_{m2} - g_{m1} + g_1 + g_2 + g_{Q3}} \qquad (7)$$

Based on the RLC model, the resonant frequency of the DAI is given by:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L - r_s^2 C_p - r_s L G_p}{L^2 C_p}}$$

$$\approx \frac{1}{2\pi}\sqrt{\frac{2g_{m2}^2 + g_{m3}(g_{m1} - g_{m2}) - g_{m1}g_{m2}}{C_{gs2}^2 + C_{gs2}(C_{gs1} + C_{gs3})} - \frac{(g_{m3} - g_{m2})^2}{(C_{gs2} + C_{gs3})^2}} \qquad (8)$$

- If the frequency f is much lower than the resonant frequency f_{res}, the RLC model will become inductive.

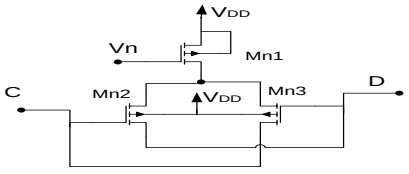
The quality factor of DAI is defined as the ratio of the imaginary part to the real part of input impedance of DAI:

$$Q_0 \Big/ \omega < \omega_{res} = \frac{L\omega}{r_s(G_p r_s + 1) + L^2 G_p^2 \omega^2} \approx \frac{(C_{gs2} + C_{gs3}) g_{m2}^2 \omega}{(g_{m3} - g_{m2})(g_{m3}(g_{m2} - g_{m1}) + g_{m1} g_{m2}) + (C_{gs2} + C_{gs3})^2 (g_{m2} - g_{m1}) \omega^2} \quad (9)$$

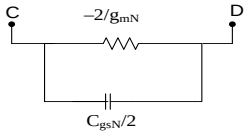
Unfortunately, this structure of DAI doesn't exhibits high-Q at switching frequency (≈100 Khz) [8]

4. Q-enhancement of active inductor

The low Q value at medium frequency can be boosted by adding negative impedance converter (NIC).
Fig.3 shows a simple NIC circuit, it's a cross connected differential pair [9],[10].



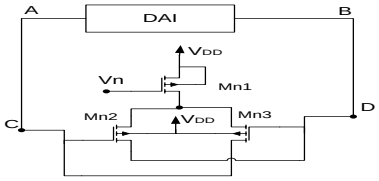
(a)



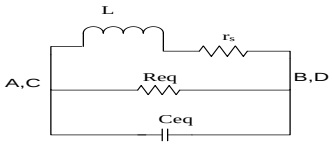
(b)

Fig.3 (a) Schematic of simple NIC. (b) Small signal equivalent circuit.

If we assume that the two transistors M_{n2} and M_{n3} are the same size, the negative differential resistance is $-2/g_{mN}$ (can be tuned by V_n), and the parallel capacitance is $C_{gsN}/2$.
By parallel connecting it to the DAI as shown in Fig.4 (a), and the RLC model equivalent is shown in Fig.4 (b).



(a)



(b)

Fig. 4 (a) Schematic of DAI with high-Q at medium frequency. (b) RLC model equivalent circuit.

With:

$$C_{eq} = C_p + \frac{C_{gsN}}{2}$$

$$R_{eq} = R_p \,//\, \frac{-2}{g_{mN}}$$

The self-resonant frequency becomes:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L - r_s^2 C_{eq} - r_s L G_{eq}}{L^2 C_{eq}}} = \frac{1}{2\pi}\sqrt{\frac{G_m}{(C_{gs2} + C_{gs3})(2C_{gs1} + 2C_{gs2} + C_{gsN})} - \frac{(g_{m3} - g_{m2})^2}{(C_{gs2} + C_{gs3})^2}} \quad (10)$$

With

$$G_m = 2g_{m2}(2g_{m2} - g_{m1}) + g_{mN}(g_{m3} - g_{m2}) + 2g_{m3}(g_{m1} - g_{m2})$$

We operated at frequency much lower than the resonant frequency.
The Q-enhancement value is:

$$Q_{enh}(\omega) \Big/ _{\omega << \omega_{res}} = \frac{R_{eq} L\omega}{r(r + R_{eq}) + L^2\omega^2} = \frac{(C_{gs2} + C_{gs3}) g_{m2}^2 \omega}{(g_{m3} - g_{m2})(g_{m3} g_{m2} - (g_{m1} + \frac{g_{mp2}}{2})(g_{m3} - g_{m2})) + (C_{gs2} + C_{gs3})^2 (g_{m2} - g_{m1} - \frac{g_{mp2}}{2})\omega^2} \quad (11)$$

To maximize Q_{enh} at switching frequency, the transistor parameters can be properly chosen such that the negative resistance of the NIC ($-2/g_{mN}$) compensates for the loss from G_p and r_s at the frequency interest.

$$real\left[\frac{1}{r_s + jL\omega}\right] + G_p - \frac{g_{mN}}{2} = 0$$

As a result, a peak Q factor can be achieved at:

$$\omega_{Q_{max}} = \frac{1}{C_{gs2} + C_{gs3}} \sqrt{\frac{(g_{m3} - g_{m2})(g_{m3}^2 - 2g_{m3} g_{m2})}{g_{m2} - g_{m1} - \frac{g_{mp2}}{2}}} \quad (12)$$

To optimize the efficiency of BC, the transistor parameters can be chosen such that the peak Q factor frequency is few hundred kHz (switching frequency).

5. Model of Buck converter with a high Q differential active inductor:

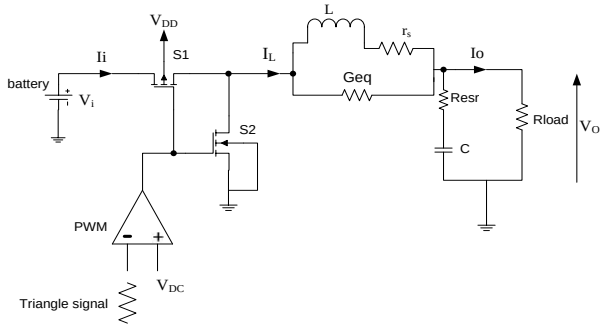


Fig.5 Buck converter with differential active inductor.

Fig.5 shown a BC with DAI and NIC, operated at frequency lower that resonant frequency [11].
The current through the active inductor can be expressed as:

$$I_L = I_{D1} - I_{D2} \qquad (13)$$

In terms of the on duty cycle is:

$$I_L = \frac{I_{D1}}{D} = \frac{I_{D2}}{1-D} \qquad (14)$$

I_L equal to the dc output current I_o, I_{D1} is the dc component of the first switch S_1 current (equal to the dc input current I_i), I_{D2} is the dc component of the second switch S_2 current.
The switches current are:

$$i_{D1} = \begin{cases} \frac{\Delta i_L}{DT} t + I_L - \frac{\Delta i_L}{2} & For\ 0<t \le t_{on} \\ 0 & For\ t_{on} < t \le T \end{cases} \qquad (15)$$

$$i_{D2} = \begin{cases} 0 & For\ 0<t \le t_{on} \\ -\frac{\Delta i_L}{(1-D)T}(t-DT) + I_L + \frac{\Delta i_L}{2} & For\ t_{on} < t \le T \end{cases} \qquad (16)$$

Where: $\Delta i_L = A I_L \frac{(1-D)}{L f_s}$ is the peak-to-peak ripple current of the inductor, and $A = \frac{R_N R_P R_L}{R_L(R_N + R_P) + R_N R_P}$

The rms values of the switches current are obtained as:

$$I_{D1rms} = \sqrt{\frac{1}{T}\int_0^{t_{on}} i_{D1}^2 dt} = I_L\sqrt{D(1+k_I^2)} \qquad (17)$$

$$I_{D2rms} = \sqrt{\frac{1}{T}\int_{t_{on}}^{T} i_{D2}^2 dt} = I_L\sqrt{(1-D)(1+k_I^2)} \qquad (18)$$

Where: $k_I = \frac{\Delta i_L}{\sqrt{12} I_L} = A\frac{(1-D)}{\sqrt{12} f_s L}$ (19)

The power loss in the MOSFETS is found as:

$$P_{r_{ds1}} = r_{ds_1} I_{D1}^2 \frac{(1+k_I^2)}{D} \qquad (20)$$

$$P_{r_{ds2}} = r_{ds_2} I_{D2}^2 \frac{(1+k_I^2)}{(1-D)} \qquad (21)$$

As r_{DS1} and r_{DS2} are the MOSFET on- resistance.
The rms value of the active inductor current is:

$$I_{Lrms} = \sqrt{\frac{1}{T}\int_0^T i_L^2 dt} = I_L\sqrt{(1+k_I^2)} \qquad (22)$$

The power loss in the active inductor is obtained:

$$P_L = \frac{r_s R_{éq}}{r_s + R_{éq}} I_{Lrms}^2 \qquad (23)$$

The current through the filter capacitor is approximately equal to the ac component of the inductor current and is given by:

$$ic = \begin{cases} \frac{\Delta i_L}{DT} t - \frac{\Delta i_L}{2} & for\ 0<t \le DT \\ -\frac{\Delta i_L}{(1-D)T}(t-DT) + \frac{\Delta i_L}{2} & for\ DT < t \le T \end{cases} \qquad (24)$$

The rms value of the capacitor current is:

$$I_{crms} = \sqrt{\frac{1}{T}\int_0^T i_c^2 dt} = k_I I_L \qquad (25)$$

The power loss in the filter capacitor is:

$$P_{Resr} = R_{esr} I_{crms}^2 = R_{esr} k_I^2 I_L^2 \qquad (26)$$

One can estimate the efficiency of the buck converter:

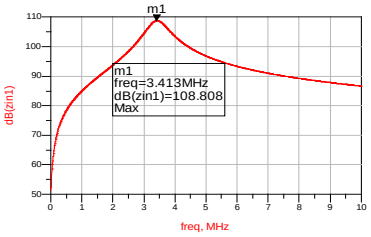
$$\eta = \frac{V_o I_o}{V_i I_i} = \frac{1}{1 + \frac{[Dr_{DS1} + (1-D)r_{DS2} + r_L](1+k_I^2) + R_{esr}k_I^2}{R_{load}}} \qquad (27)$$

As:

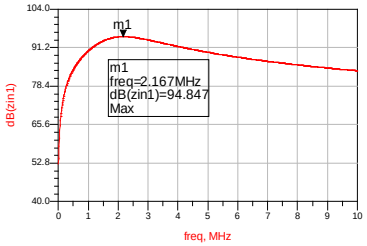
$$r_L = \frac{r_s R_{éq}}{r_s + R_{éq}} .$$

6. SIMULATION RESULTS

The DAI was simulated in 0.18um CMOS technology. Fig.6 shows the variation of input admittance versus frequency of the DAI. Current dissipation of the DAI is 14uA, DAI without NIC resonance at 3.41MHz, and the DAI with NIC resonance at 2.16MHz.



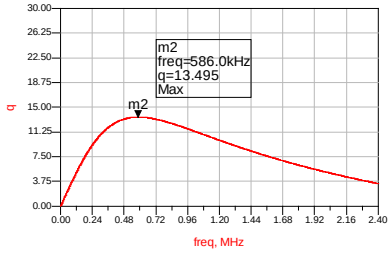
(a)



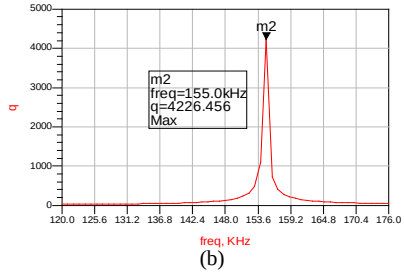
(b)

Fig.6. Variation of input admittance of the DAI: (a) without NIC. (b) With NIC.

Fig.7 shows the quality factor versus frequency of the DAI. Where the DAI with NIC presented a maximum quality factor Qd≈4226 at 155 KHz.



(a)

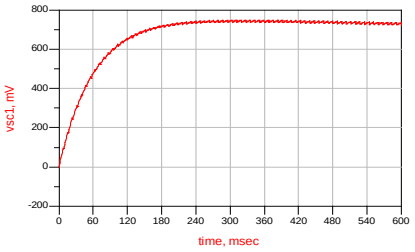


(b)

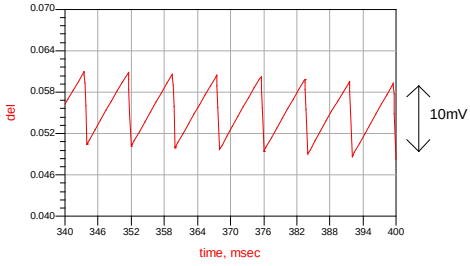
Fig.7 Quality factor of the DAI: a) without NIC. (b) With NIC.

The BC with DAI and NIC is supplied with an input voltage of 1V and switching frequency of 155 kHz.
Fig.8 (a) represents the output voltage of this BC, and the output ripple voltage is shown in Fig.8 (b).
Thus the ripple of output voltage is expressed as follows [5]: $$\Delta V_o = A\frac{(V_i - V_o)D}{16LCf_s^2} = \frac{\Delta i_L}{8Cf_s}$$

and the efficiency of this BC equal: $$\eta = \frac{V_o I_o}{V_i I_i} = 0.75$$



(a)



(b)

Fig.8 Buck converter with differential active inductor: (a) Output voltage of the Buck converter. (b) Output ripples voltage of 10mV.

Fig.9 is the transient response of output voltage with variation of capacitance in the LP filter. The recovery time is in the order of 30ms for capacitance C=100nF and 180ms for C=1uF.

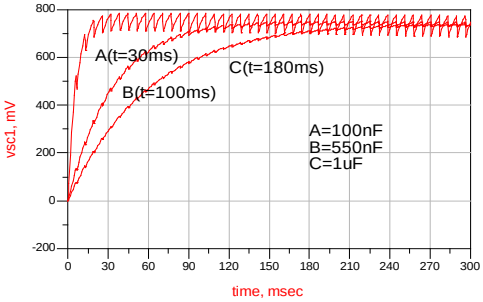


Fig.9 Transient response of output voltage with variation capacitance in the LP filter.

7. Conclusion

In this paper we simulated a buck converter implemented in a 0.18um technology with CMOS differential active inductor paralleled with active negative resistor which uses a minimum number of transistors and presented a high quality factor. The measurement results show that the Buck converter is supplied with an input voltage of 1V and switching frequency of 155 kHz, an low power consumption (14uW), an output voltage of 740mV and output ripple voltage of 10mV.
Due to the use of active inductors, no distributed elements or spiral inductors are required. A significant reduction in chip area can be achieved.
The present work proves that the DAI aren't only suitable for RF applications, but also at medium frequency.

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