

# Review of ASITIC (Analysis and Simulation of Inductors and Transformers for Integrated Circuits) Tool to Design Inductor on Chip

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## Abstract

Passive elements such as inductors, capacitors, and transformers have the potential to improve the performance of key RF building blocks. Despite the fact about their utilization, is not only the need of proper modeling of electrostatic and magneto-static effects, but also is the coupling of electromagnetic parasitic substrate. In this paper, a custom-built computer-aided-design tool called ASITIC, “Analysis and Simulation of Inductors and Transformers for Integrated Circuits” is illustrated, which is vastly used for analysis, design, and optimization of passive devices. This tool allows circuit and process engineers to design and optimize the geometry of passive devices and the process parameters to meet electrical specifications optimally. Since, the losses in the passive devices determine the achievable gain and power dissipation, thus optimization of such passive devices is now becoming an integral part in the design of such building blocks.

**Keywords:** ASITIC, Inductor-on-Chip, CAD, LNA, Parasitic Capacitance.

## 1. Introduction

The wireless communication revolution has spawned a revival of interest in the design and optimization of radio transceivers. Passive elements such as inductors, capacitors, and transformers play critical part in today’s transceivers. Until recently, passive devices, especially in integrated form, played relatively minor role in Si integrated circuits in comparison with active devices such as transistors. The most important reason for this can be endorsed as the size difference. Through the era, active devices are continuously shrinking and occupying less and less chip area whereas passive devices occupying large space. At low frequencies, circuit designers employed simulated passive devices as much

as possible to make their products more compact and reliable [2]. While it was possible to fabricate small values of capacitance on-chip, at the same time inductors were virtually impossible due to the large physical area required to obtain sufficient inductance at a given frequency. This was compounded by the losses in the substrate which made it virtually impossible to fabricate high quality devices. Small Si die were desirable to keep costs low in order to improve reliability since larger die results in lower yields [3].

When passive devices were needed, usually they were connected externally onboard rather than on-chip. This is possible as long as few external components are needed and the package parasitics are negligible in comparison with the external electrical characteristics of the device.

In order to design inductor on chip, a custom CAD tool, ASITIC was used to analyze a wide variety of test structures such as square spirals, polygon spirals, coupled spirals and transformers [1].

In this paper, In this paper, a custom-built computer-aided-design tool called ASITIC, “Analysis and Simulation of Inductors and Transformers for Integrated Circuits” is illustrated, which is vastly used for analysis, design, and optimization of passive devices. With the introduction in Section-1, Applications of ASITIC tool for passive devices is explored in Section-2. The ASITIC overview and organization is discussed in Section-3 & 4. Optimization of Parameters for Optimal Inductor Performance is covered in Section-5 with a design example explored in Section-6. Finally the conclusion remarks are mentioned in Section-7.

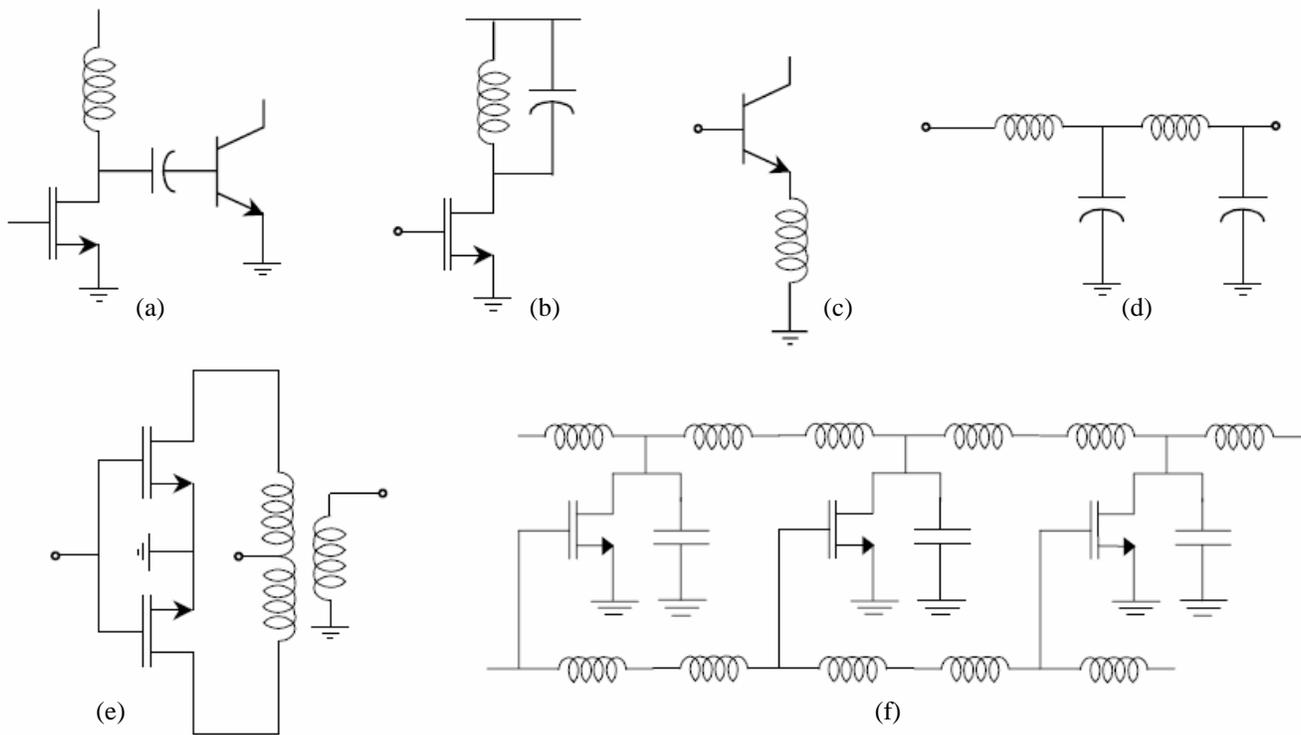


Fig 1: Applications of passive devices in Si IC building blocks. (a) Impedance matching. (b) Tuned load. (c) Emitter degeneration. (d) Filtering. (e) Balun. (f) Distributed amplifier. [2].

## 2. Applications of Passive Devices

Passive devices, such as inductors and transformers, play an integral part in the performance of circuit building blocks, especially at high frequency. Inductors can be avoided at lower frequencies by using simulated inductances employing active devices. Simulated inductors are more difficult to realize at higher frequencies as active device gain drops. In addition, simulated inductors have finite dynamic range, require voltage headroom to operate, and inject additional noise into the circuits. These limitations place a severe restriction on their application, especially in highly sensitive analog building blocks. In Fig. 1, we can observe several common applications of inductors, capacitors, and transformers in wireless building block circuits.

In Fig. 1(a) we see a narrow-band impedance matching example. Here the input impedance of the second transistor is matched to an optimal impedance value desired by the driving transistor. For instance, in a power amplifier the input impedance of a large output stage device is low due to the capacitance, and to obtain sufficient power gain, this low impedance is transformed into a larger value. Impedance matching allows circuit designers to obtain minimal noise, maximum gain,

minimal reflections, and optimal efficiency when designing circuit building blocks such as low-noise amplifiers (LNAs), frequency-translation circuits (mixers), and amplifiers.

In Fig. 1(b) we see an  $LC$  tuned load. A tuned load can take the place of a resistive load to obtain gain at high frequency. The advantages are clear as an  $LC$  passive is less noisy than a resistor, consumes less voltage headroom, and obtains larger impedance at high frequency. A resistive load is always limited by the  $RC$  time constant which limits the frequency response. Tuned loads are also critical components of oscillators. The  $LC$  tank tunes the center frequency of the oscillator and the intrinsic  $Q$  allows the tank to oscillate with minimal power injection (and hence noise) from the driving transistor.

In Fig. 1(c) an inductor is used as a series-feedback element. Series feedback can be used to increase the input impedance, stabilize the gain, and lower the non-linearity of the amplifier. By using an inductor in place of a resistor, less voltage headroom is consumed, and less additional noise is injected into the circuit. The inductance can also be used to obtain real input impedance at a particular frequency, thus providing an impedance match at the input of the amplifier.

In Fig. 1(d) inductors and capacitors are used to realize a low-pass filter. Filters of this type are superior to active filter realizations such as gm-C or MOSFET-C filters as they operate at higher frequencies, have higher dynamic range due to the intrinsic linearity of the passive devices, and inject less noise while requiring no DC power to operate.

In Fig. 1(e) we see a center-tapped transformer serving as a balun, a device which converts a differential signal into a single-ended signal to drive external components. Differential operation is advantageous in the on-chip environment due to the intrinsic noise rejection and isolation. Off-chip components, such as SAW filters, though, are single-ended and a balun is needed to convert external single-ended signals to on-chip differential signals. Finally, in Fig. 1(f) we see inductors and capacitors forming an artificial transmission line in a distributed (traveling-wave) amplifier. Since the LC network acts like a transmission line, it has a broadband response. A wave propagating on the gate-line is amplified and transferred onto the drain line. If the wave speed on the drain line matches the gate line, the signals on the drain line add in phase and the drain line delivers power into a matched load [2].

### 3. ASITIC Overview

ASITIC is the amalgamation of the key concepts and techniques as described in [2], assembled into a user-

friendly and efficient software tool. ASITIC allows one to move easily between the electrical, physical, geometric, and network domains. In the electric domain, the device is described by the relevant electrical parameters, such as inductance, capacitance, quality-factor  $Q$ , and self-resonant frequency. In the physical domain, the device is described by the constituent material properties, such as the thickness, conductivity, permittivity, and permeability. In the geometric domain, the device is described by its physical dimensions and relative position in the volume of the integrated circuit. In the network domain, the device is described by network two-port parameters.

In short, the goal of ASITIC is to create an easy-to-use numerical software package for the analysis and design of passive devices over the Si substrate. The key objective is accuracy, flexibility, and efficiency [2].

### 4. ASITIC Organization

Fig. 2 is a block diagram of ASITIC. ASITIC is composed of several software modules that interact over clearly defined interfaces. The user interacts with ASITIC at the top level through the graphical and text interface. The technology file describes the pertinent process parameters such as substrate layer thickness, conductivity, and permittivity data, as well as metal thickness and conductivity values.

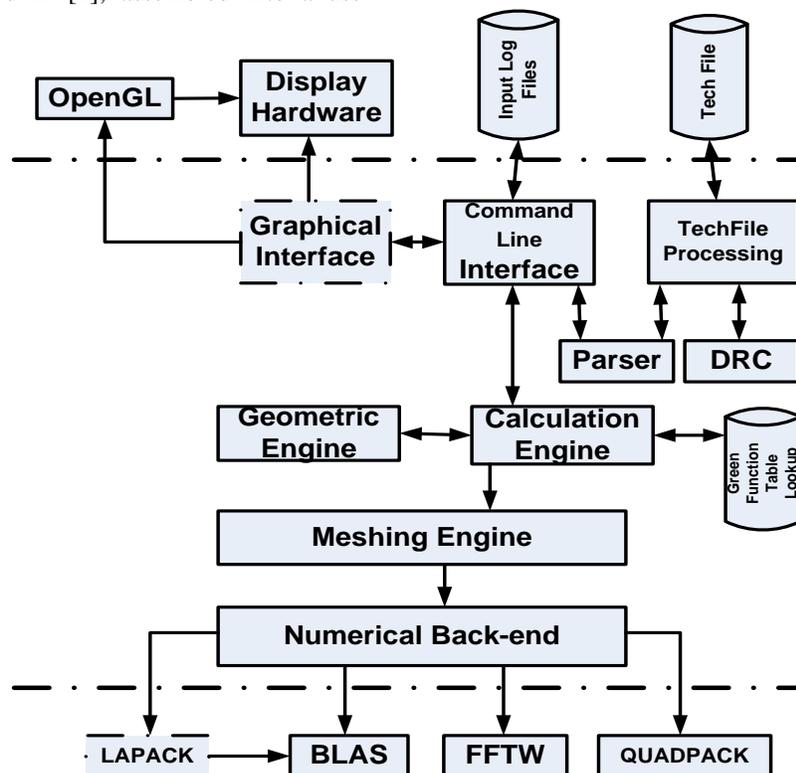


Fig. 2. Block Diagram of the ASITIC Modules [2]

By means of ASITIC commands, users are able to create, modify, optimize, and analyze passive devices. The top ASITIC layers rely on the geometry and calculation engines to create and analyze structures. The geometry engine is able to synthesize structures such as square and polygon spirals. The calculation engine is able to quickly analyze the structures and display electrical parameters. The calculation engine in turn depends on the meshing engine to convert geometric representations of devices into electrically small geometric sub elements used for the analysis. The numerical back-end modules convert the electrical sub-elements into algebraic equations through numerical integration. These numerical computations are accelerated by several software libraries such as Basic Linear Algebra Subroutines (BLAS), Linear Algebra Package (LAPACK) [4], an extension of (LINPACK), and Fastest FFT in the West (FFTW) [5], and the numerical integration package QUADPACK [6].

Another important element in ASITIC is graphical interface. ASITIC is capable of displaying devices in two and three dimensions. The three-dimensional representations produced with OpenGL are highly useful in understanding and verifying complex multi-metal structures. Physical dimensions can be distorted to more easily visualize the structure. For instance, the z-direction can be scaled to clearly delineate closely spaced metal layers.

### 5. Optimization of Parameters for Optimal Inductor Performance

Much is known about the optimization of the technological parameters of a process for optimal inductor performance [7]. Thicker or higher conductivity metal improves the quality factor at low frequencies, whereas a higher resistivity substrate and thicker oxide help to isolate the device from the substrate at high frequencies. The optimization of the geometry of inductors and transformers, though, is more difficult. Even for simple structures, such as square spirals, there are several parameters to optimize, including the area of the spiral, the metal width and spacing, and the number of turns. Not much can be said in general since the optimal geometry depends on the frequency of operation. [8]

For instance, at low frequency, one usually uses the minimum spacing available to maximize magnetic coupling, but at high frequency, proximity effects and magnetic coupling favor a larger value of spacing [9]. This is illustrated in Fig. 3, where we plot the resistance of a typical spiral using two values of spacing. Similar considerations apply to the area of the spiral and the number of turns. At lower frequencies, large areas allow wider metal widths to meet a given inductance at lower values of series resistance and therefore higher but at high frequencies, this is dominated by the substrate and smaller

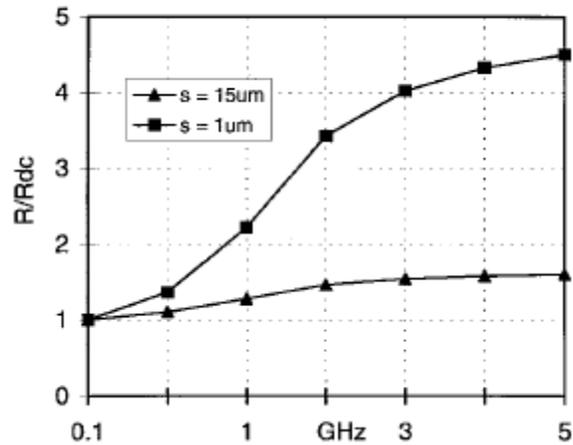


Fig. 3 Normalized spiral resistance as a function of frequency

areas are favorable. This is doubly true for highly conductive substrates that suffer from eddy-current losses at high frequency [9].

Thus, the optimization of such structures must be done carefully on a case-by-case basis. To aid this process, a custom tool has been developed. The techniques presented in this paper have been collected into Analysis and Simulation of Inductors and Transformers for IC's (ASITIC), to a user friendly computer-aided-design (CAD) tool designed to aid the RF circuit designer in the designing, optimizing, and modeling of the spiral inductor and transformers. The tool is flexible, allowing the user to tradeoff between speed and accuracy. For example, ASITIC can be used to quickly search the parameters space of an inductor optimization problem.

### 6. Design Example

A 2GHz LC tank will be designed as a part of LC oscillator. C value is given as 3pF.

- Find L value.
- Design a spiral inductor with L value ( $\pm 5\%$  range) obtained from (a) using ASITIC. Optimize the design parameters: W, S, D and N to get a high Q ( $Q_{min} = 5$ ). Show L, Q,  $f_{SR}$  value obtained from simulation.
- Show the layout.
- Give a lumped circuit model.

SOLUTION:

- LC tank oscillation frequency is given as 2GHz.

$$\omega_{osc} = \frac{1}{\sqrt{LC}} \dots\dots(1)$$

$$L = \frac{1}{\omega_{osc}^2 \cdot C} \dots\dots (2)$$

$$\therefore L = \frac{1}{(2 \times \pi \times 2 \times 10^9)^2 \cdot (3 \times 10^{-12})}$$

$L = 2.11 \text{ nH}$  is desired.

- (b)  $L = 2.11 \text{ nH}$  ( $\pm 5\%$ ) is used as input parameter. Several design parameters are tried to get high  $Q$  and  $f_{SR}$  values. Final design has

Parameters:

$W = 19 \mu\text{m}$ ,

$S = 1 \mu\text{m}$ ,

$D = 200 \mu\text{m}$ ,

$N = 3.5$

Resulting Inductor:

$L = 2.06 \text{ nH}$ ,

$Q = 7.11$ ,

$f_{SR} = 9.99 \text{ GHz @ } 2 \text{ GHz}$

This design is acceptable as  $Q > Q_{min}$  and  $f < f_{SR}$ .

- (c) ASITIC generates the layout automatically as mentioned in Fig-4. It can be saved and imported to be used in other tools such as Cadence, ADS and Sonnet.

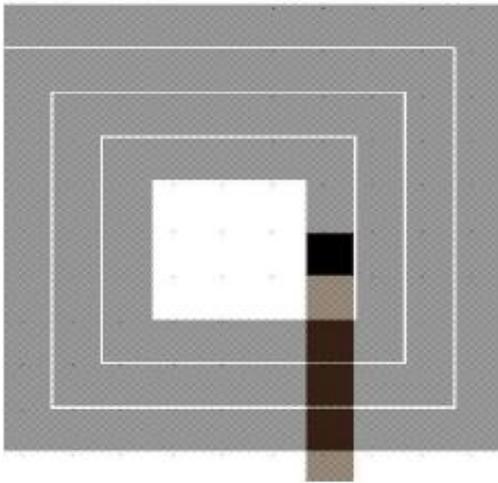


Fig. 4. Square Spiral Inductor Layout generated through ASITIC Tool

- (d) Analysis in ASITIC gives a  $\pi$  model as mentioned in Fig.5.  $\pi$  model is usually not symmetrical and this can be used for differential configuration where none of the two ports is ac-grounded.

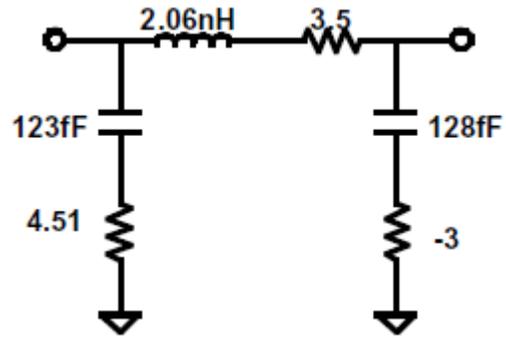


Fig. 5.  $\pi$ -model produced through ASITIC data

## 7. Conclusion

The ASITIC tool is found to be very useful in designing passive devices on chip, like inductors, and transformers. It also helps to optimize the parameters so as to increase the speed and efficiency of the circuit.

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