Dependence of Substrate Resistance of RF MOSFET on the Performance of LNA at 60 GHz

Sari S, Karthigha Balamurugan and Jayakumar M

Communication Engineering Research Group, Electronics and communication Engineering, Amrita VishwaVidyapeetham, Coimbatore, Tamil Nadu, India

Abstract

Operations in the 60 GHz band have many potential advantages compared to other unlicensed frequency bands including the availability of large bandwidth (7 GHz) and high-transmission power levels. In order to utilize this plentiful resource, it is necessary to study the MOSFET devices at 60 GHz for developing high efficiency low noise amplifier and oscillators. The modeling is mainly based on substrate resistance to improve the operating frequency. π -type substrate resistance model of RF MOSFETs are used as composite model for MOSFET. In composite model, core transistor is modeled using BSIM4 and substrate network is added to it. The functionality of this composite model is verified by comparing with that of conventional MOSFET. To study the impact of substrate network, a 60 GHz LNA is constructed. Conventional LNA is designed first and later MOSFET in that LNA are replaced with composite model and comparing performances in both the cases. Within the range of designs, the impact of π -type substrate resistance network on noise figure, maximum available gain, maximum stable gain, high frequency noise and stability characteristics of the LNA are significant and reported.

Keywords: BSIM4, Composite model, millimeter-wave LNA, Millimeter-wave technology, radio frequency modeling.

1. Introduction

CMOS technology has become a popular choice for realizing transistors for RF applications. Due to the continuous downscaling of CMOS technology, RF performance of CMOS transistors have been improved considerably over the years. An important issue of RF devices is the non-availability of compact RF models to accurately predict the RF characteristics at high frequencies, including the millimeter wave range. For modeling RF MOSFETs, the substrate resistance is important at frequencies that are close to or higher than threshold frequency f_T . Especially, the substrate resistance significantly affects the small-signal output characteristics of MOSFETs at high frequency.

The impact of gate finger shape and substrate contact ring shape and its position, on the substrate resistance (R_{sub}), f_T , sand f_{max} of 45 nm CMOS devices is studied. R_{sub} increases

by 64% in going from a ring contact to a one sided contact [1]. In this work they concluded that high frequency noise, power gain and power added efficiency is independent of moderate changes in substrate resistance. But at the same time, high frequency unilateral power gain and fmax strongly depends on Cgb and Rsub. A layout level substrate resistance extraction was carried out in [2], shows a scalable model of substrate resistances for RF MOSFETs with a bar-type body contact was presented. This model describes the output admittance (Y₂₂₎ characteristics of RF MOSFETs with different layout conditions. An equation for substrate resistance, in which R_{sub} is a function of number of fingers, was also formulated. This model was valid upto 50 GHz. π -type substrate resistance model was considered in [3] where substrate resistance was extracted analytically using three port Y parameter analysis which was verified upto 110 GHz. In [4-5], substrate resistance was extracted and modeled as a single lumped resistor. This resistor was scalable with geometric parameters and depended on biasing conditions. R_{sub} was extracted at V_{gs}=0V, where intrinsic components of MOSFET are negligibly small. The dependence of body contact on substrate resistance shows that R_{sub} is proportional to the distance to body contact and is inversely proportional to the width of the body contact of MOSFET [6]. Substrate resistance extracted from ring type body contact is a parallel combination of the R_{sub} of vertical and horizontal type devices. C_{gd0} and C_{id} were also extracted in [6]. Need for highly accurate Y-parameter measurement data, a physics-based high frequency MOS equivalent circuit, and a complete direct parameter extraction for the equivalent circuit were demonstrated in [7]. High frequency behavior of MOS devices is determined by both intrinsic and extrinsic parasitic components and the NQS effect was included in RF model [8].

Composite model proposed by I. M. Kang et.al., [3] is good for 60 GHz range since that model has valid up to 110 GHz. Fig.1 shows the equivalent circuit of MOSFET with π -type substrate resistance model when V_{gs}=0V. Here, the gate-to-source and gate-to-drain extrinsic capacitances are represented by C_{gs0} and C_{gd0}, respectively. C_{gb} is the



capacitance between gate and body. C_{js} and C_{jd} represent the junction capacitance of source and drain. R_{sb} , R_{db} , and R_{dsb1} - R_{dsb2} represent resistances between source and body, resistance between drain and body and resistance between source and drain through bulk, respectively. Here, the gate resistance is neglected, to make the extraction of substrate resistance easy.

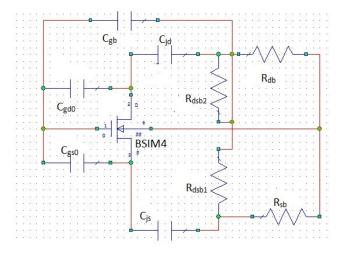


Fig. 1 Composite model of MOSFET

In this paper, core transistor was modeled using BSIM4 and the substrate network was added as shown in Fig.1. Influence of this substrate network on the performance was studied by constructing a low noise amplifier. The LNA is verified with and without composite sub circuit model to prove the influence of substrate network on the overall performance of the device at 60 GHz and load capacitance of 1pF in 0.13 μ m CMOS technology.

2. A 60 GHz LOW NOISE AMPLIFIER (LNA)

Performance requirements for a millimeter-wave LNA are power gain, noise figure, linearity, stability, impedance matching, power dissipation, bandwidth and design robustness. 60 GHz LNA is not much different from other RF LNA's in terms of design methodologies. Three fundamental differences of 60 GHz design compared to lower frequency design, is that transistors (1) are designed to operate much closer to their cutoff frequencies, (2) are designed to operate with signals with smaller wavelengths, and (3) are designed with parasitic elements which represent a much larger portion of the total impedance or admittance on a given node. Transistors operating close to f_T have less gain and higher noise figure. LNA reduces effect of noise from subsequent stages of the receiver chain even though it injects noise directly into the received signal. Thus major duty of an LNA is to boost the desired signal power while adding a little noise and distortion. So that recovery of this signal is possible in the later stages in the system. LNA is a class- A amplifier for which the bias point is more or less at the centre of maximum current or voltage capability of the device used, since RF current and voltage are sufficiently small relative to bias point. LNA plays an important role in the receiver design especially to maintain required signal-to-noise ratio of the system at extremely low power levels. In addition to this, LNA amplifies the received signals with large signal levels without introducing any distortions, which helps to avoid channel interference.

Simultaneous requirement for high gain, low noise figure, good input and output matching and unconditional stability make an LNA designing to be a challenging one. In order to make a circuit unconditionally stable a certain reduction in gain is needed. High third-order intercept point (IP3) requires higher current draw. But for lowest noise figure demands lower current levels.

Advantages of common-gate stage are wideband input matching and less sensitivity to parasitics. It has high noise figure. As the frequency increases parasitic transistor capacitance C_{gs} comes into play, which degrade amplifier performance. In narrow band application, a shunt inductor is added in the input of transistor to resonate with C_{gs} to achieve impedance matching in the designed frequency. Advantages of Common gate LNA are robustness against process and electrical variation due to lowest Q factor of resonant circuit, and better reverse isolation and stability due to missing of the C_{gd} path from input to the output.

Cascode LNA with inductive degeneration is a good choice for CMOS applications where noise figure is a critical issue [12] [13]. Noise figure can be improved by increasing bias current for a given unit-gain frequency, and by increasing gm for a given quality factor (Q). As bias current reduces, C_{gs} decreases which leads to a higher Q. But drawbacks of matching network are circuit shows high dependence to components variation, series inductor will be present in the input matching circuit and transistor M_2 is added in the circuit to improve stability but due to cascode topology noise will be introduced by M_2 .

2.1 LNA design

Purpose of L_s , and L_g are input impedance matching, to set the resonant frequency $f_0=60$ GHz and to increase output gain by tuning respectively. L_d works as a bandpass filter along with load capacitance C_L . M_3 , M_2 , C_B and R_{bias} are to



bias transistor which forms current mirror with transistor M_1 , to isolate tuned input from output to increase reverse isolation (to reduce Miller capacitance C_{gd}), and to reduce equivalent noise current respectively. Size of M_3 is chosen to reduce power consumption. R_{bias} should be large enough so that its equivalent current noise can be neglected. Size of M_3 and M_2 are same so that they can share common drain area. Conventional 60GHz LNA is shown in fig.4.

Optimal input matching and minimum noise figure is given by [13]

$$G_{opt} = \alpha \omega C_{gs} \sqrt{\frac{\delta (1 - |C|^2}{5\gamma}}$$
(1)

Where c is cross correlation coefficient, α is a constant nearly equal to unity, γ is the coefficient of channel thermal noise and δ is the coefficient of gate noise. The minimum noise figure is given as

$$F_{\min} = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma C (1 - |C|^2)}$$
(2)

Optimum transistor width is obtained when noise figure of the LNA is optimized for a given power which is higher than the global minimum noise figure (NF_{min}).

$$W_{opt} = \frac{1}{3\omega_0 L_{eff} C_{ox} R} \tag{3}$$

$$C_{gs} = \frac{2}{3} W_{M1} L_{eff} C_{ox}$$
 (4)

$$g_{M1} = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)_{M1} I_{DM1}}$$
(5)

$$\omega_T = \frac{g_{M1}}{C_{gs1}} \tag{6}$$

$$L_{S} = \frac{R_{S}}{\omega_{T}}$$
(7)

$$L_{s} + L_{g} = \frac{1}{\omega_{0}^{2} C_{gsl}}$$
(8)

$$L_d = \frac{1}{\omega_0^2 C_L} \tag{9}$$

Where W is the transistor width, L_{eff} is effective channel length, C_{ox} is oxide capacitance of the transistor. g_{M1} is the trans-conductance of M_1 transistor. ω_0 is the centre frequency of LNA, here $f_0=60$ GHz.

To study the influence of composite model of MOSFET, existing MOSFETs were replaced with composite model in the same LNA without altering other components. From the various plots of noise figure, maximum stable gain, minimum noise figure and various port parameters, the influence of substrate network on overall performance of the device is obtained.

3. RESULTS AND DISCUSSION

3.1 Composite Model

To In the composite model of MOSFET [3], core transistor was modeled using BSIM4 and high frequency substrate components were added externally shown in Fig.1. This model for number of fingers, $N_f = 16$, was reproduced with the same parameters as mentioned in [3].

In this paper output characteristic of this composite model is compared with the conventional NMOS with the same geometric parameters for both. Output characteristic of composite model is shown in Fig.2. From the obtained output characteristic, it is clear that, here this characteristic is similar to conventional NMOS output characteristic. Both are showing same relationship between parameters, thus composite model was verified using HSPICE.

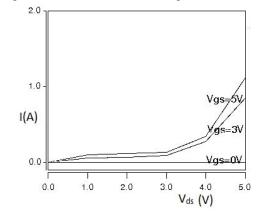


Fig. 2 $I_d\text{-}V_{ds}$ characteristics of composite model of NMOS with W=1.8 $\mu m,$ L=.13 μm and N_f =16

3.2 60 GHz Low Noise Amplifier

Eq. (1-9) are used for designing millimetre-wave low noise amplifier.Fig.3.is the conventional millimeter-wave LNA. Various components of LNA and their values are given below

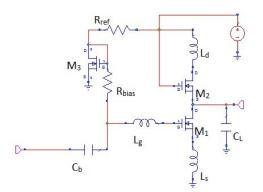


Fig.3 Conventional LNA for millimeter wave applications

Table	1.	INA	Design	parameters
raute	1.	LINA	DUSIGI	parameters

Component	Value
R _{ref}	2ΚΩ
R _{bias}	2ΚΩ
R _S	21.2867 KΩ
C _B	.402Pf
Lg	.2526nH
L _d	7.04pH
Ls	.102pH
CL	1pF

The performance of millimetre-wave LNA is analyzed by considering noise figure, minimum noise figure, maximum stable gain and stability circles of input and output using AWR Design Environment. The ' Δ 'in the plots represent the conventional LNA and the '×' represents the modified LNA. To study the impact of composite model on these responses, replace MOSFET in LNA with new parasitic model.

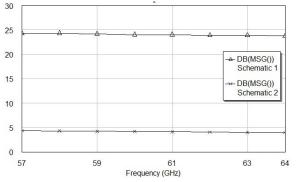


Fig.4 Maximum stable gain (dB) of conventional LNA (Schematic 1) and that of modified LNA (Schematic 2)

In Fig.4, the simulated maximum stable gain (MSG) versus frequency is shown. At a frequency of 60 GHz, maximum stable gain of conventional LNA was 24.02 dB and that of modified LNA (.i.e., MOSFET is replaced with composite model) was 4.2dB. For an ideal LNA MSG should be high. In that aspect conventional LNA is good. But practically at RF range resistance parasitic will come into play, this is the reason for reducing MSG in modified LNA.

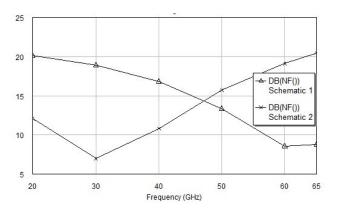


Fig. 5 Noise Figure (dB) of conventional LNA (Schematic 1) and that of modified LNA (Schematic 2)

In Fig.5, the simulated noise figure versus frequency was shown for both cases. At a frequency of 60 GHz, obtained noise figure for conventional millimeter-wave LNA was 8.55 dB and that of modified LNA was 19.13 dB. Fig.6 shows the minimum noise figure plotted versus frequency. In ideal case, noise figure of an LNA should be 0dB. But practically at the operating frequency LNA shows lower noise figure. Minimum noise figure for conventional LNA and that of modified LNA are 0.387 dB and 7.391 dB, respectively. Fig.12 shows the noise circle for both cases. In the noise circle minimum and actual noise figure for each frequency of both LNA are plotted.

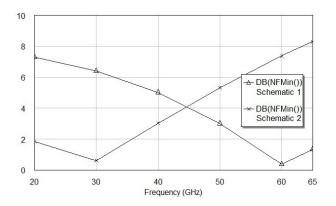


Fig. 6 Minimum Noise Figure (dB) of conventional LNA (Schematic 1) and that of modified LNA (Schematic 2)



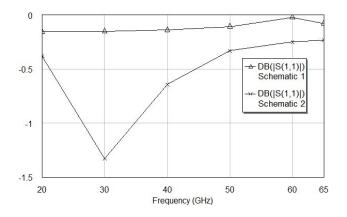


Fig. 7 S₁₁ (dB) of conventional LNA (Schematic 1) and that of modified LNA (Schematic 2)

The S-parameter extraction is done for both conventional and modified LNA. Extracted S parameters of both LNA's are shown in fig.7-10. S_{11} & S_{22} are input and output reflection coefficients, it should be low. S_{21} (dB) is the transducer gain. S_{12} (dB) is reverse gain of an amplifier. For an ideal LNA, S_{12} is zero.

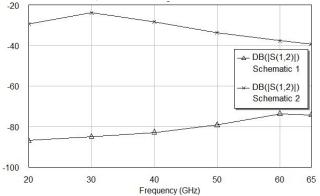


Fig.8 S $_{12}$ (dB) of conventional LNA (Schematic 1) and that of modified LNA (Schematic 2)

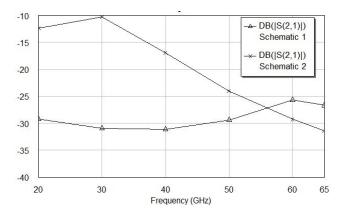


Fig. 9 S_{21} (dB) of conventional LNA (Schematic 1) and that of modified LNA (Schematic 2)

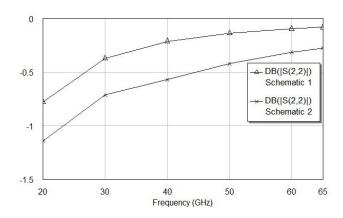


Fig. 10 S₂₂ (dB) of conventional LNA (Schematic 1) and that of modified LNA (Schematic 2)

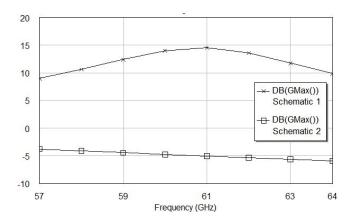


Fig. 11 Maximum Available Gain (dB) of conventional LNA (Schematic 1) and that of modified LNA (Schematic 2)

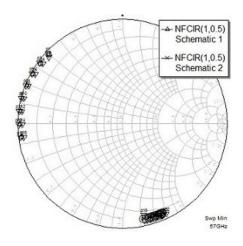


Fig. 12 Noise figure circle of conventional LNA (Schematic 1) and that of modified LNA (Schematic 2)

In Fig.11, maximum available gain was shown. Maximum available gain of conventional LNA is 14.033 dB and that of modified LNA is -4.722 dB at 60 GHz.

For the modified LNA, the centre frequency is shifted to 30 GHz. At that frequency modified LNA shows good performance like low noise figure and low minimum noise figure value.

Parameters	Conventional LNA at 60 GHz (dB)	Modified LNA at 60 GHz (dB)	Modified LNA at 30 GHz (dB)
NF	8.55	19.13	7.018
NF min	0.387	7.391	0.6075
S11	-0.0223	-0.2505	-1.321
S12	-73.77	-37.68	-23.87
S21	-25.74	-29.28	-10.28
S22	-0.097	-0.3143	-0.714
MSG	24.02	4.2	6.8
MAG	14.033	-4.74	6.79

Table 2: Performance summary of Conventional millimeter- wave LNA & Modified LNA

Conventional LNA has good performance in terms of maximum stable gain, maximum available gain and in noise figure. The inclusion of substrate network reduces the performance of conventional millimeter-wave MOSFET. Ideal case, substrate resistance can be neglected in RF design. But practically, it has strong impact on determining overall efficiency of a system containing this MOSFET. RC components in the substrate network in modified millimeter-wave LNA may be the reason for shifting of the resonating frequency from 60GHz to 30 GHz. in both the cases, substrate network won't affect the stability of LNA. For modified LNA, noise figure is good at 30 GHz.

4. Conclusions

Substrate resistance of MOSFET is very important at millimeter-wave RF CMOS technology. Output

characteristic of composite model is similar to that of conventional NMOS characteristic. For the verification of composite model a millimeter-wave LNA for 60 GHz is designed. To study the influence of substrate network on the overall performance, a comparison with and without adding substrate network on MOSFET of LNA was carried out. NF, NF_{min}, MSG, MAG, noise circles, stability circles and S-parameters are considered to compare the performance of both the LNA's. Results show that the conventional LNA performs better at 60 GHz when compared to the modified LNA. But, Modified LNA showed good performance at 30 GHz. This indicates that its centre frequency is shifted to 30 GHz from 60 GHz due to addition of substrate network. So substrate network of MOSFET cannot be neglected at millimeter-wave frequency band.

References

- [1] Usha Gogineni, Hongmei Li, Jesus A. del Alamo, Susan L. Sweeney, Jing Wang, and Basanth Jagannathan, "Effect of Substrate Contact Shape and Placement on RF Characteristics of 45 nm Low Power CMOS Devices,"IEEE J. Solid-State Circuits, vol. 45, no. 5, May 2010, pp. 998–1006.
- [2] In Man Kang, Seung-Jae Jung, Tae-Hoon Choi, HyunWoo Lee, Gwangdoo Jo,Young-Kwang Kim, Han-Gu Kim, and Kyu-Myung Choi, "Scalable Model of Substrate Resistance Components in RF MOSFETs With Bar-Type Body Contact Considered Layout Dimensions," IEEE Electron Device Lett., vol. 30, no. 4, APR. 2009, pp. 404-406.
- [3] I. M. Kang, J. D. Lee, and H. Shin, "Extraction of π -type substrate resistance based on three-port measurement and the model verification up to 110 GHz," IEEE Electron Device Lett., vol. 28, no. 5, May 2007 pp. 425–427.
- [4] J. Han, M. Je, and H. Shin, "A simple and accurate method for extracting substrate resistance of RF MOSFETs," IEEE Electron Device Lett., vol. 23, no. 7, Jul. 2002, pp. 434–436.
- [5] Jeonghu Han, Minkyu Je and Hyungcheol Shin, "Extraction of Substrate Resistances of RF MOSFETs with Various Geometries," Journal of the Korean Physical Society, vol. 42, no. 2, Feb.2003, pp. 224-228
- [6] Jeonghu Han, Minkyu Je and Hyungcheol Shin, "Physical modeling of substrate resistance in RF MOSFETs" Nanotech, vol. 2, ISBN 0-9728422-1-7, pp. 290-293, 2003.
- [7] S. H.-M. Jen, C. C. Enz, D. R. Pehlke, M. Schroter, and B. J. Sheu, "Accurate modeling and parameter extraction for MOS transistor valid up to 10 GHz," IEEE Trans. Electron Devices, vol. 46, no. 11, Nov. 1999, pp. 2217–2227.
- [8] Y. Cheng, M. J. Deen, and C. H. Chen, "MOSFET modeling for RF IC design," IEEE Trans. Electron Devices, vol. 52, no. 7, Jul. 2005, pp. 1286–1303.

- [9] Shervin Ehrampoosh and Ahmad Hakimi, "High Gain CMOS Low Noise Amplifier With 2.6 GHz Bandwidth," Proc. ICComE 2010 Int. Conference on Communication Engineering, Dec 2010, pp. 72 - 76.
- [10] M. S. Alam, "RF Modelling of deep sub-micron CMOS and heterojunction bipolar transistor for wireless communication system", Ph.D. thesis, Queen's University of Belfast, U.K., 2002.
- [11] Frank Ellinger, "26–42 GHz SOI CMOS Low Noise Amplifier," IEEE J. Solid-State Circuits, vol. 39, no.3, Mar2004, pp.522–528.

Sari S received the B.Tech. degree in electronics and communication engineering from Calicut university, India, in 2010. She is currently pursuing M.Tech degree in VLSI design at the Amrita Vishwa Vidyapeetham, Coimbatore, India. Her current research interests are parasitic extraction and modeling of millimeter-wave MOSFET, FET modeling and antenna design.

Karthigha Balamurugan received the BE degree from Bharathiar University, in 1998 and ME degree from Government College of Technology, Coimbatore, India, in 2008.She currently pursuing PhD. Her research interest is device modeling for millimeter-wave applications.

Jayakumar M received his doctorate in Microwave Electronics in 1996 from the University of Delhi. He worked in Thapar University, Patiala from 1996 to 1997 as a lecturer in Electrical and Telecommunication Engineering department. In 1997, he joined Indian Space Research Organization (ISRO), Trivandrum in the design and development of antennas for airborne vehicles and simulation of communication links for various missions. In 2001, he joined Essel group, Mumbai in the satellite bandwidth and spectrum management group for direct broadcasting satellite services. He had attended several orbit-frequency coordination meetings in ITU, Geneva for Indian DTH services. Presently working as a professor in Amrita Vishwa Vidyapeetham since 2003 involved in teaching and research in the area of millimeter wave wireless communication systems, advanced antenna designs for air borne vehicles, cylindrical microstrip antennas etc. He was the recipient of Dr. K.S.Krishnan research fellowship from the department of Atomic Energy and IEEE student award by the IEEE Magnetic Society U.S.A. He is a member and Hon. Secretary of IETE Coimbatore Center.

283

