Efficient Circuit Configuration for Enhancing Resolution of 8-bit flash Analog to Digital Convertor

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Abstract

The need constantly exists for converters with higher resolution, faster conversion speeds and lower power dissipation. High speed analog to digital converters (ADC's) have been based on flash architecture, because all comparators sample the analog input voltage simultaneously, this ADC is thus inherently fast. Unfortunately flash ADC requires $2^N - 1$ comparators to convert N bit digital code from an analog sample. This makes flash ADC's unsuitable for high resolution applications. The focus of this paper is on efficient circuit configuration to enhance resolution of available 8-bit flash ADC, while maintaining number of comparators only 256 for 12 bit conversion. This technique optimizes the number of comparator requirements. In this approach, an 8-bit flash ADC partitions the analog input range into 256 quantization cells, separated by 255 boundary points. An 8-bit binary code 00000000 to 11111111 is assigned to each cell. The Microcontroller decides within which cell the input sample lies and assigns a 12-bit binary center code 000000000000 to 111111111111 according to the cell value. The exact 12-bit digital code is obtained by successive approximation technique. In this paper the focus will be on all-around efficient circuit for enhancing resolution of 8-bit Flash ADC. It is shown that by adopting this configuration, we can obtain 12-bit digital data just using 256 comparators. Therefore this technique is best suitable when high speed combined with high resolution is required. An experimental prototype of proposed 12-bit ADC was implemented using Philips P89V51RD2BN Microcontroller. Use of Microcontroller has greatly reduced the hardware requirement and cost. An ADC result of 12-bit prototype is presented. The results show that the ADC exhibits a maximum DNL of 0.52LSB and a maximum INL of 0.55LSB.

Keywords: *Flash ADC, Microcontroller, DAC, Sample and Hold. Successive approximation.*

1. Introduction

Analog-to-digital converters (ADCs) are critical building blocks in a wide range of hardware from radar and electronic warfare systems to multimedia based personal computers and work stations [1]. The need constantly exists for converters with higher resolution, faster conversion speeds and lower power dissipation. An N-bit flash architecture uses 2^N-1 comparators, where N is the stated resolution. Flash converters often include one or two additional comparators to measure overflow conditions [2].

All comparators sample the analog input voltage simultaneously. This ADC is thus inherently fast. The Parallelism of the flash architecture has drawbacks for higher resolution applications. The number of comparators grows exponentially with N, in addition, the separation of adjacent reference voltages grows smaller exponentially and consequently this architecture requires very large IC's. It has high power dissipation.

The conventional pipelined architecture has been widely employed to meet the required performance in this arena due to properly managed trade-offs between speed, power consumption and die area [3-5]. Among a variety of pipelined ADCs, the multi bit-per-stage architecture is more suitable for high resolution, as the single bit- per stage structure requires more stages, high power consumption and larger chip area [6]. However the multi bit-per-stage architecture has a relatively low signal processing speed due to reduced feedback factor in the closed – loop configuration of the amplifiers. In switched capacitor type multiplying digital-to-analog converters (MDACS) used in conventional pipelined ADCs, the mismatch between capacitors limits the differential non linearly (DNL) of ADCs. This is because each DNL step is defined by the random process variation of each unit capacitor value. A common centroid geometry layout technique can improve this capacitor matching for DNL, but it cannot have an effect on random mismatch [7]. Naturally, increasing the capacitor size can directly improve the capacitor matching accuracy, but at the added cost of increased load capacitance. This means the amplifiers would dissipate more power or the ADC sampling speed would have to be reduced. Two step Flash converters are popular for conversion resolutions in the

8-12 bit range where optimized designs can achieve low power dissipation and small silicon area for implementation [8, 9]. However, beyond such resolution, the area and power dissipation of two-step flash ADC's nearly double for each additional bit of resolution [10]. There are many different architectures like pipelined convertor [11, 12], successive approximation convertor [13, 14], Sigma-Delta convertor [15], folding ADC's [16], reported recently for high speed applications. But these architectures have significant amount of complexity. In this paper a simple technique is proposed to enhance resolution of flash ADC's.   The prototype ADC based on this technique uses only 256 comparators instead of 4096 comparators normally required in the flash ADC's for 12-bit resolution.

2. Flash ADC

Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal. Flash ADCs are suitable for applications requiring very large bandwidths. However, these converters consume considerable power, have relatively low resolution, and can be quite expensive. This limits them to high-frequency applications that typically cannot be addressed any other way. Typical examples include data acquisition, satellite communication, radar processing, sampling oscilloscopes, and high-density disk drives.

2.1 Architectural Details

Flash ADCs are made by cascading high-speed comparators. Figure 1 shows a typical flash ADC block diagram. For an N-bit converter, the circuit employs 2^N-1 comparators. A resistive-divider with 2^N resistors provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a 1 when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is 0. Thus, if the analog input is between V_{X4} and V_{X5}, comparators X_1 through X_4 produce 1s and the remaining comparators produce 0s. The point where the code changes from ones to zeros is the point at which the input signal becomes smaller than the respective comparator reference-voltage levels. If the analog input is between V_{X4} and V_{X5}, comparators X_1 through X_4 produce 1s and the remaining comparators produce 0s.
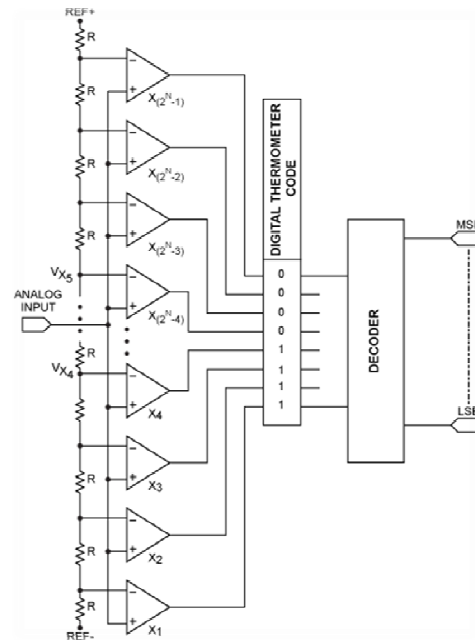This architecture is known as thermometer code encoding.

Figure 1. Flash ADC architecture.

This name is used because the design is similar to a mercury thermometer, in which the mercury column always rises to the appropriate temperature and no mercury is present above that temperature. The thermometer code is then decoded to the appropriate digital output code.

The comparators are typically a cascade of wideband low-gain stages. They are low gain because at high frequencies it is difficult to obtain both wide bandwidth and high gain. The comparators are designed for low-voltage offset, so that the input offset of each comparator is smaller than an LSB of the ADC. Otherwise, the comparator's offset could falsely trip the comparator, resulting in a digital output code that is not representative of a thermometer code. A regenerative latch at each comparator output stores the result. The latch has positive feedback, so that the end state is forced to either a 1 or a 0.

3. Successive approximation ADC

Successive approximation ADCs are widely used for high resolution 10-12bit, medium speed 5MS/s, low-power, low-cost applications such as automotive, factory automation, and pen digitizer applications. [17-21]. Successive approximation ADCs with improved performance, lower cost, and higher reliability can make a significant impact in industry.

3.1 Configuration of successive approximation ADC

A conventional successive approximation   ADC consists

of a track-hold circuit, a comparator, a DAC, successive approximation   logic and time-base circuits Figure 2 shows a typical block diagram of successive approximation ADC. The track-hold circuit, and ensuring linearity of DAC input-output characteristics, is the most critical parts of the design. Usually a ring counter is used in the time-base circuitry to provide accurate timing signals.

3.2 Operation of successive approximation ADC

The successive approximation   ADC operates according to a binary search algorithm as follows:
The track-hold circuit samples and holds the voltage of the analog input Vin (full-scale input is Vref).
The comparator compares the voltages of Vin (held by the track-hold circuit) and Vref /2 (where Vref /2 is generated by the DAC).
In case Vin > Vref /2:
The comparator outputs logic "1".
The comparator then compares the voltage Vin with (3/4)Vref (where (3/4)Vref is generated by the DAC).
If Vin > (3/4)Vref, then (7/8)Vref is used for the next comparison. Else if Vin < (3/4)Vref, then (5/8)Vref is used.
This binary search continues in this manner.
In case Vin < Vref /2:
The comparator outputs logic"0".
The comparator then compares the voltages Vin with (1/4)Vref (where (1/4)Vref is generated by the DAC).
If Vin > (1/4)Vref, then (3/8)Vref is used for the next comparison. Else if Vin < (1/4)Vref, then (1/8)Vref is used.
The successive approximation ADC performs N comparisons,   and   then   outputs   a   digital   value corresponding to the N-bit binary comparison result. Figure 3 illustrates the case for N = 4.
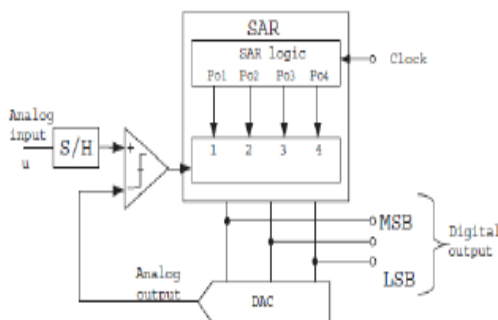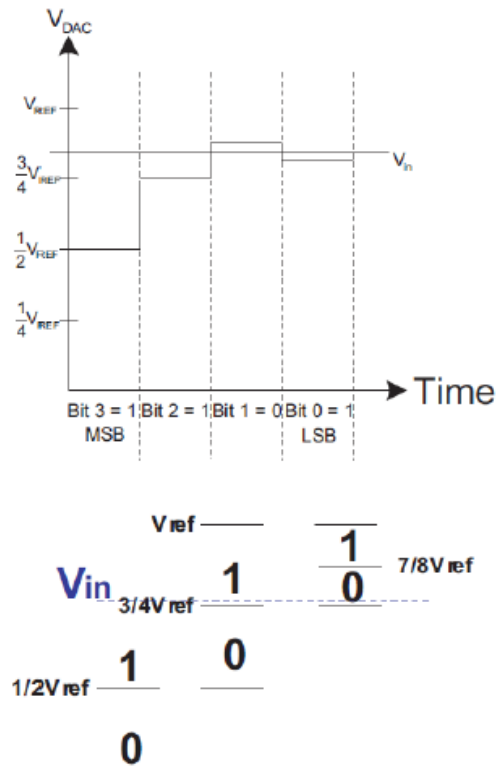

Figure 2: Block diagram of Successive approximation ADC

Figure 3: Operation of Successive approximation ADC

4. Proposed ADC Architecture

Flash ADC's are promising for high Speed applications. However, these ADC's are unsuitable for high resolution applications.   The   number   of   comparators   grows exponentially with resolution, and consequently this architecture requires very large IC's and it has high power dissipation. The ADC based on our technique enjoys the benefit of employing only 256 comparators instead of 4096 comparators normally required in conventional 12-bit flash architecture while maintaining the advantage of high speed. The block diagram of the 12-bit ADC using proposed technique is illustrated in Figure-4. The ADC consists of an input sample and hold amplifier (SHA),   8-bit flash ADC,   12-bit DAC, 8-bit Microcontroller 8051, 8:16 bit MUX/DEMUX switch and some extra supporting circuit blocks. 8-bit flash ADC, partitions input range into 256-quantization cells, separated by 255 boundary points. An 8-bit binary code 00000000 to 11111111 is assigned to each cell. The Microcontroller decides within which cell the input sample lies and assigns a 12-bit binary center code 000000000000 to 111111111111 according to the cell value. Table 1 summarizes Binary code and corresponding center value of each cell. The exact   12-bit digital code for analog sample is obtained by successive approximation technique.

Table 1: Binary code and center value of cells

Cell No. (N)	Maximum Voltage of the cell(V_N)	Binary Code for the cell (B_N)	Center Value Binary Code of the Cell (MB_N)
0	0.0195	00000000	000000001000
1	0.0391	00000001	000000011000
2	0.0586	00000010	000000101000
3	0.0781	00000011	000000111000
4	0.0977	00000100	000001001000
5	0.1172	00000101	000001011000
253	4.9609	11111101	111111011000
254	4.9805	11111110	111111101000
255	5.0000	11111111	111111111000

4.1 Circuit implementation

The block diagram of the 12-bit ADC is as shown in Figure 4. The microcontroller port 0 is used as input port, which gets the 8-bit code from 8-bit flash ADC; corresponding center value 12-bit binary code of a particular cell is loaded into the accumulator and R0. Port 2 is used as output port, connected to 12-bit DAC through 8:16 bit switch to obtain analog signal equivalent to digital count in register A and R0, which is compared with an analog input voltage V_{IN}. Equivalent 12-bit digital code for analog input signal is obtained by successive approximation technique. The conversion algorithm is similar to the binary search algorithm. First, the reference voltage of a particular cell, Vref (DAC) provided by DAC is set to $V_N / 2$ to obtain the MSB, where V_N is the maximum cell voltage of a particular cell and N is cell number. After getting the MSB, successive approximation convertor moves to the next bit with $V_N/4$ or $3/4*V_N$ depending on the result of the MSB. If the MSB is "1", then Vref(DAC) = $\frac{3}{4}*V_N$, otherwise Vref(DAC) =$V_N/4$. This sequence will continue until the LSB is obtained. Figure 5 shows how the reference voltages are implemented for analog signal sample lies in the third cell (V3/2=038H). Note that 15/16*V3 (03FH) is the largest reference voltage and 1/16*V3 (031H) is the smallest reference voltage. To get a 12-bit digital output, 4 comparisons are needed. Finally 12-bit digital code is available at 8:16 bit switch.
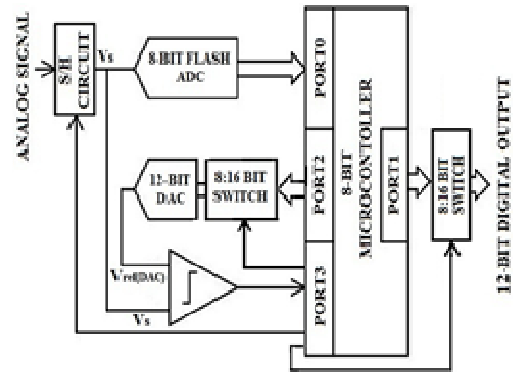

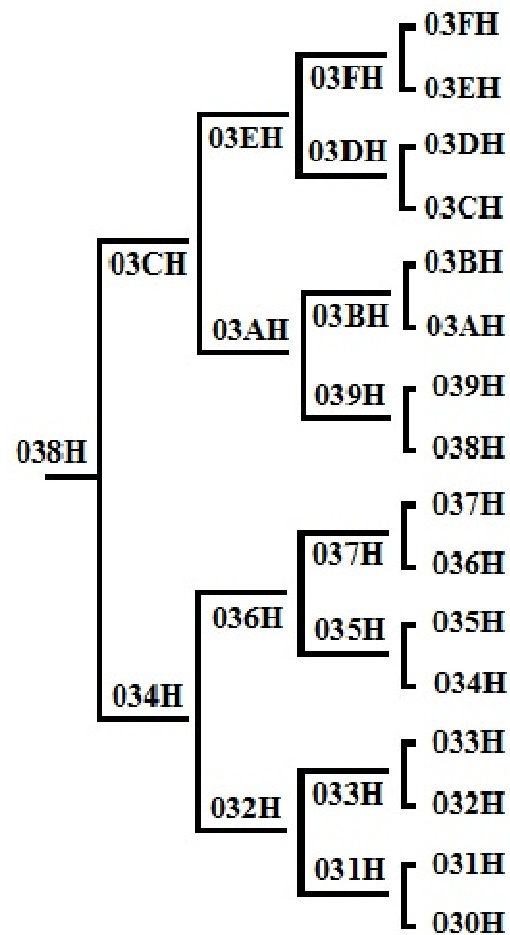Figure 4: Block diagram of 12-bit ADC

Figure 5: Reference voltage tree in successive approximation technique

Software for implementing successive approximation converter in Microcontroller is written in assembler code and converted to hex code by assembler software. Hex codes are transferred to microcontroller by programmer. Flowchart of software is shown in Figure 6.
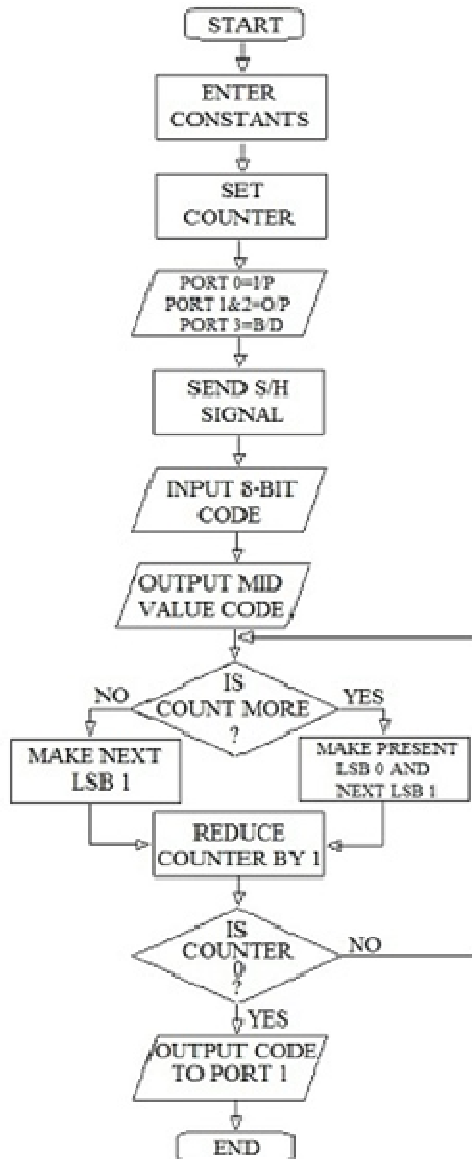
Figure 6: Flowchart of software

5. Measured result

An experimental prototype of 12-bit ADC using proposed technique was designed and developed using Philips P89V51RD2BN. The working functionality of the ADC has been checked by generating a ramp input going from 0 to 5V (full scale range of the ADC). Digital codes have been obtained correctly, going from 0 to 4095 for 12-bit at the output, indicating that the ADC's working is functionally correct.

Both the differential and integral nonlinearities (DNL and INL) were measured over 2^{12} output codes by applying slowly varying full scale range ramp as input to the proposed ADC, which completes the full scale range in 4095 steps .The values of the each code are compared with

ideal value and store the difference value. The results show that the ADC exhibits a maximum DNL of 0.52 LSB and a maximum INL of 0.55LSB as shown in the Figures 7(a) and 7(b).
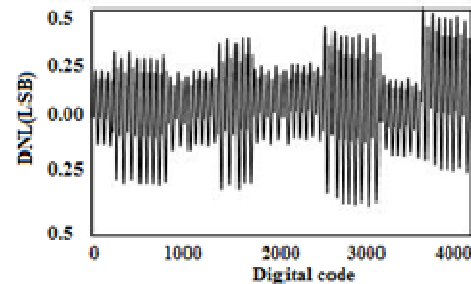

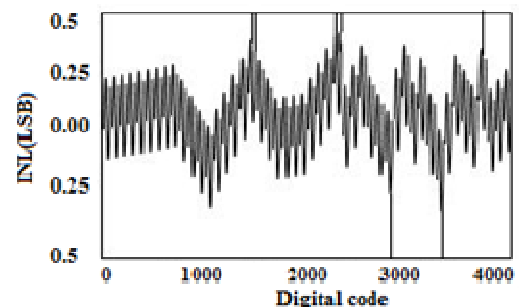Figure 7(a): Differential Non Linearity Versus output Code

Figure 7(b): Integral Non Linearity Versus output Code

6. Conclusion

We have presented a simple and effective technique for enhancing resolution of 8-bit flash ADC. This technique would be effective in a large number of high speed controls and signal processing applications such as hard-disk-drive read Chanel and wireless receivers. Although these applications are most often implemented with flash convertors, but these ADC's demands larger power. And also, the ADC die area and power dissipation increase exponentially with resolution, limiting the resolution of such ADC's less than 10bits. The main conclusion is that although Flash convertors provide high conversion rates, required power dissipation of these ADC's are large. Also, resolution beyond 10bits these ADC's become prohibitively expensive and bulky. Proposed technique provides high enough conversion speed for high speed applications, with less power dissipation even beyond 10bit resolution. Implementation of successive approximation algorithm using Microcontroller has reduced the hardware requirement and cost. Proposed technique uses only 256 comparators for 12-bit resolution.

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